

What is claimed is:

1. A method for reducing sparkle artifacts in a liquid crystal imager, comprising the steps of:  
 dividing a video signal for a picture into a higher brightness level signal and a lower brightness level signal;  
 slew rate limiting said lower brightness level signal;  
 delaying said higher brightness level signal to match a processing delay incurred by said slew rate limiting; and,  
 combining said slew rate limited lower brightness level signal and said delay matched higher brightness level signal to generate a modified video signal less likely to result in sparkle artifacts in said imager.

2. The method of claim 1, comprising the step of dividing said video signal in accordance with a transition between lower and higher gain portions of a gamma table associated with said imager.

3. The method of claim 1, wherein said dividing step comprises the steps of:  
 selecting a brightness level threshold;  
 comparing successive input brightness levels of said luminance signal to said selected threshold;  
 for each said input brightness level greater than said threshold in said comparing step, assigning to said higher brightness level signal a brightness level equal to a difference between said greater input brightness level and said threshold and assigning to said lower brightness level signal a brightness level equal to said threshold; and,  
 for each said input brightness level less than said threshold in said comparing step, assigning to said higher brightness level signal a brightness level equal to zero and

15 assigning to said lower brightness level signal a brightness  
16 level equal to said input brightness level.

1 4. The method of claim 3, comprising the steps of:  
2 assigning to said higher brightness level signal a  
3 brightness level equal to zero if said input brightness level  
4 is equal to said threshold; and,  
5 assigning to said lower brightness level signal a  
6 brightness level equal to said input brightness level if said  
7 input brightness level is equal to said threshold.

1 5. The method of claim 1, comprising the step of  
2 delaying said higher brightness level signal to compensate for  
3 a delay incurred in said slew rate limiting.

1 6. The method of claim 1, comprising the steps of:  
2 applying said sparkle reducing steps to a luminance  
3 signal for said picture;  
4 delaying chrominance signals for said picture; and,  
5 generating a plurality of video drive signals from said  
6 modified luminance signal and said delayed chrominance  
7 signals.

1 7. The method of claim 6, comprising the steps of:  
2 applying said sparkle reducing steps to at least one of  
3 said video drive signals; and,  
4 delaying all non-sparkle-reduced video drive signals.

1 8. The method of claim 1, comprising the steps of:  
2 generating a plurality of video drive signals from  
3 luminance and chrominance signals;  
4 applying said sparkle reducing steps to at least one of  
5 said video drive signals; and,  
6 delaying all non-sparkle-reduced video drive signals.

1           9. The method of claim 8, comprising the step of  
2 applying said sparkle reducing steps to each of said video  
3 drive signals.

1           10. The method of claim 7 comprising the step of  
2 independently selecting slew rate limits for said slew rate  
3 limiting steps.

1           11. A circuit for reducing sparkle artifacts in a liquid  
2 crystal imager, comprising:  
3 means for dividing a video signal for a picture into a  
4 higher brightness level signal and a lower brightness level  
5 signal;  
6 means for slew rate limiting said lower brightness level  
7 signal;  
8 means for delaying said higher brightness level signal to  
9 match a processing delay incurred by said slew rate limiting;  
10 and,  
11 means for combining said slew rate limited lower  
12 brightness level signal and said delay matched higher  
13 brightness level signal to generate a modified video signal  
14 less likely to result in sparkle artifacts in said imager.

1           12. The circuit of claim 11, wherein said dividing means  
2 comprises:  
3 a register for storing a selected threshold value;  
4 a comparator for comparing successive input brightness  
5 levels of said luminance signal to said selected threshold  
6 value;  
7 an algebraic circuit for subtracting said threshold value  
8 from every one of said input brightness levels greater than  
9 said threshold;

10 a clipping circuit for limiting to said threshold value  
11 every one of said input brightness levels greater than said  
12 threshold value

13 a first gate for propagating a zero value brightness  
14 level for every one of said input brightness levels less than  
15 said threshold value;

16 a second gate for propagating said input brightness level  
17 for every one of said input brightness levels less than said  
18 threshold; and,

19 said higher brightness signal is formed by outputs from  
20 said algebraic circuit and said first gate and said lower  
21 brightness level signal is formed by outputs from said  
22 clipping circuit and said second gate.

13. The circuit of claim 12, wherein:

2 said higher brightness level signal is formed by said  
3 output of said first gate when said input brightness level is  
4 equal to said threshold value; and,

5 said lower brightness level signal is formed by said  
6 output of said second gate when said input brightness level is  
7 equal to said threshold value.

1 14. The circuit of claim 11, wherein said threshold  
2 value relates to a transition between lower and higher gain  
3 portions of a gamma table associated with said imager.

1 15. The circuit of claim 11, wherein said higher  
2 brightness level signal is delayed to match a delay incurred  
3 by operation of said slew rate limiting means.

1 16. The circuit of claim 11, wherein said video signal  
2 is a luminance signal, and further comprising:  
3 means for delaying chrominance signals for said picture;  
4 and,

means for generating a plurality of video drive signals from said modified luminance signal and said delayed chrominance signals.

17. The circuit of claim 16, comprising:

means for dividing at least one of said video drive signals into a higher brightness level video drive signal and a lower brightness level video drive signal;

means for slew rate limiting said lower brightness level video drive signal;

means for delaying said higher brightness level video drive signal to match a processing delay incurred by said slew rate limiting; and,

means for combining said slew rate limited lower brightness level video drive signal and said delay matched higher brightness level video drive signal to generate a modified video drive signal resulting in a further reduction of declination in said imager.

18. The circuit of claim 17, wherein said brightness level thresholds for said luminance signal dividing means and said video drive signal dividing means are independently selectable.

19. The circuit of claim 17, wherein slew rate limits for said slew rate limiting means are independently selectable.

20. The circuit of claim 17, comprising:

respective means for dividing, slew rate limiting, delaying and combining each one of said video drive signals; and,

each of said luminance signal dividing means and said video drive signal dividing means having independently

7 selectable brightness level thresholds and each of said slew  
8 rate limiting means having independently selectable slew rate  
9 limits.

1 21. A circuit for reducing sparkle artifacts in a liquid  
2 crystal imager, comprising:

3 a decomposer for dividing a video signal for a picture  
4 into a higher brightness level signal and a lower brightness  
5 level signal;

6 a slew rate limiter for processing said lower brightness  
7 level signal, said slew rate limited lower brightness level  
8 signal being delayed;

9 a delay circuit for said higher brightness level signal  
10 matched to said processing delay in said slew rate limiter;  
11 and,

12 an algebraic circuit for combining said slew rate limited  
13 lower brightness level signal and said delay matched higher  
14 brightness level signal, and generating a modified video  
15 signal less likely to result in sparkle artifacts in said LCOS  
16 imager.

1 22. The circuit of claim 21, wherein said decomposer  
2 circuit has a selectable threshold value.

1 23. The circuit of claim 22, wherein said threshold  
2 value is related to a transition between lower and higher gain  
3 portions of a gamma table associated with said imager.

1 24. The circuit of claim 22, wherein said higher  
2 brightness level signal is delayed to match a delay incurred  
3 by said slew rate limiter.

1 25. The circuit of claim 21, wherein said video signal  
2 is a luminance signal, and further comprising:

3 delay circuits for delay matching chrominance signals for  
4 said picture with said modified luminance signal; and,  
5 a color space converter for generating a plurality of  
6 video drive signals from said modified luminance signal and  
7 said delay matched chrominance signals.

1 26. The circuit of claim 25, further comprising:  
2 a further decomposer for dividing at least one of said  
3 video drive signals into a higher brightness level video drive  
4 signal and a lower brightness level video drive signal;  
5 a further slew rate limiter for said lower brightness  
6 level video drive signal;  
7 a further delay circuit for delaying said higher  
8 brightness level video drive signal to match a processing  
9 delay incurred by said slew rate limiter; and,  
10 a further algebraic circuit for combining said slew rate  
11 limited lower brightness level video drive signal and said  
12 delay matched higher brightness level video drive signal to  
13 generate a modified video drive signal, resulting in a further  
14 reduction of declination in said imager.

1 27. The circuit of claim 26, wherein said decomposer and  
2 said further decomposer have independently selectable  
3 brightness level thresholds.

1 28. The circuit of claim 26, wherein said slew rate  
2 limiter and said further slew rate limiter have independently  
3 selectable slew rate limits.

1 29. The circuit of claim 26, comprising:  
2 respective decomposers, slew rate limiters, delay  
3 circuits and algebraic circuits for processing each one of  
4 said video drive signals; and,

5        each of said decomposers having independently selectable  
6        brightness level thresholds.